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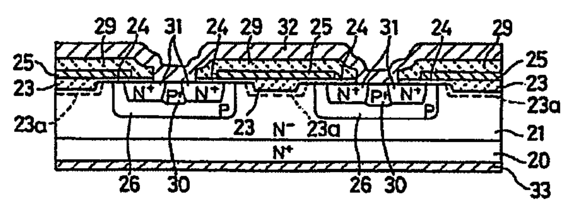
(54) **A vertical-type MOSFET and method of fabricating the same.**

(57) A vetical-type MOSFET having high switching capabilities is shown. The high switching speed is facilitated by reduce the capacity between the drain and gate without providing adverse effects on the advantages based on the double diffusion method. The FET is constituted so that the distance between gate electrode and drain region is larger than the distance between the gate electrode and well region functioning as channels.



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TITLE OF THE INVENTION

A vertical-type MOSFET

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device for a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), and more particularly to a so called "vertical-type MOSFET" having high switching speed.

Recently, it is strongly required to simplify driving circuits and integrate them thereby to allow the power supply voltage of the circuits to be lowered. So as to realize this requirement, there is a tendency that a power MOSFET, particularly a vertical-type MOSFET which has low ON resistance (referring to resistance at a time of "ON") is suitable for power switching element.

Referring to Fig. 1, there is shown typical cell or chip structure of a prior art vertical-type MOSFET. The term "vertical" is derived from the fact that currents flow in the vertical direction of the transistor cell. The prior art vertical MOSFET cell is fabricated in accordance with following fabrication processes;

a) An N^--type layer of low impurity concentration is epitaxially grown on a drain substrate 1 of low resistivity comprised of an N^+-type silicon wafer of high impurity concentration to form a drain region 2 of high resistivity, which defines a semiconductor wafer 4 together with the drain substrate 1.

b) An insulating coating 3 for a gate is formed on a principal surface of the drain region 2 of high resistance by a thermal oxidation method, and then a polysilicon film constituting a gate electrode 5 is formed on the surface thereof.

c) The polysilicon film is selectively removed using photo-etching techniques to open source windows. Thereafter, under the condition that the remaining polysilicon film serves as a mask, through the opened source windows thus formed, there are successively formed by a double diffusion method a well region 6 functioning as channels, and source and well contact regions 7, 8

which diffuse concentrically within the well region 6 from the center thereof towards the outer periphery thereof.

d) After the double diffusion process is completed, a source electrode 10 is formed on the upper surface of the gate electrode 5 through an insulating film 9 by vacuum deposition. Further, a drain electrode 11 is formed on the rear side of the drain substrate 1 of low resistivity. Thus, the prior art vertical-type MOSFET cell shown in Fig. 1 is completed.

In the prior art vertical-type MOSFET to which the above-described method is applied, both the well region 6 and the source region 7 are formed by the double diffusion method. For this reason, when a large number of transistor elements are fabricated on the silicon wafer, following advantages will accrue. Namely, uniformity in characteristics of each transistor can be obtained. The production yield can be remarkably improved. The transistor device can be small-sized.

However, with the double diffusion method, after ion implantation is effected through the source windows with the polysilicon film constituting the gate electrode serving as a mask, it is necessary to in advance coat the whole area interposed between the adjacent source windows in order to form the well region and the source region are formed by the double diffusion method.

For this reason, the completed transistor cell has the geometrical configuration in which the polysilicon film exists still in area corresponding to the upper surface of the drain region, which area correspond to areas or portions except for the upper surface of the channel region required for the gate electrode. From a structual view point, the gate electrode and the drain region are spaced each other solely through the thin insulating film interposed therebetween. Accordingly, this results in large capacity between the drain and gate electrodes. Further, the capacity serves as a feedback circuit from the output of the switching element to the input thereof, thereby making it impossible or difficult to effect switching at a high

speed.

SUMMARY OF THE INVENTION

with the above in view, it is an object of the invention to provide a vertical-type MOSFET making it possible to extremely reduce or lessen the capacity between the drain and the gate to effect switching at a high speed.

It is another object of the invention to provide a vertical-type MOSFET wherein the prior art double diffusion method is directly applicable when fabricating the MOSFET of the invention in spite of a provision of an improvement for high switching capability thereof, thereby making it possible to fabricate it at a low cost without lowering the production yield even if transistor device elements are required to be integrated in a densely packed manner, which is advantages based on the double diffusion method in a following manner.

These and other objects and advantages are accomplished based on a vertical-type MOSFET wherein the structure thereof is formed so as to increase the effective distance between a gate electrode film and a drain region in a following manner.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross sectional view illustrating a typical structure of a prior art vertical-type MOSFET,

Figs. 2(A) to 2(I) are cross sectional views illustrating a first embodiment of a vertical-type MOSFET element according to the present invention, each showing fabricating processes thereof,

Figs. 3(A) to 3(G) are cross sectional views illustrating a second embodiment of a vertical-type MOSFET element according to the present invention, each showing fabricating processes thereof, and

Figs. 4(A) to 4(H) are cross sectional view illustrating a third embodiment of a vertical MOSFET element according to the present invention, each showing fabricating processes thereof.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to Figs. 2, there is shown the first embodiment of

the invention. A example of fabricating processes or steps of an n-channel vertical-type MOSFET according to the first embodiment will be described with reference to Figs. 2(A) to 2(I).

Initially, as shown in Fig. 2(A), the method comprises the step of epitaxially growing an N^--type monocrystalline silicon layer 21 of high resistivity, having low donor impurity concentration N_D of about $2x10^{15}$atoms/cm^3 and thickness of about 15μm, on a drain substrate 20 of low resistivity comprising an N^+-type monocrystalline silicon wafer of high concentration of donor impurities N_D of about $1x10^{18}$atoms/cm^3 to form a drain region 21 of high resistivity. A semiconductor wafer 10 is defined by the drain substrate 20 and the drain region 21.

As shown in Fig. 2(B), the method further comprises the steps of covering or coating areas or portions, in which well regions for forming channels will be formed, with a resist 22 on a upper surface of the drain region 21 of high resistivity, effecting dryetching the surface of opened window portions formed in the resist 22 by about 1μm to form recess portions 21a, and thereafter removing the resist 22.

As shown in Fig. 2(C), the method further comprises the steps of depositing a silicon oxide film 23 including therein arsenic (As) having molecular concentration of about 3% by a CVD (Chemical Vapour Deposition) method so that the thickness thereof is 1μm on the whole surface thereof, and removing the silicon oxide film 23 except for the recess portions 21a by photo-etching techniques. In this instance, the silicon oxide films 23 filled in the recess portions 21a is formed in such a manner that each upper end is projected from the surface of the drain region 21. More particularly, the silicon oxide films 23 having gradually inclined peripheral edges projected from the surface of the drain region 21.

As shown in Fig. 2(D), the method further comprises the steps of forming a silicon oxide film 24 for a gate on the surface of the drain region by thermal oxidation so that the thickness thereof is approximately 10^2nm (1,000Å), and forming a

polysilicon layer constituting a gate electrode 25 on the upper surface thereof by a CVD method. In this instance, N-type impurities of arsenic (As) contained in the silicon oxide film 23 provided within the recess portions 21a diffuses due to the thermal oxidation mentioned above. As shown by dotted lines, N^+-type regions 23a of high concentration are formed along the interface between the periphery of the silicon oxide film 23 and the drain region 21 of high resistivity.

As shown in Fig. 2(E), the method further comprises the steps of selectively removing by photo-etching techniques the portions of the polysilicon layer in which the well region will be formed, except for gate electrodes 25, effecting boron ion (B^+) implantation with the gate electrode portions 25 serving as a mask, and effecting heat treatment for 24 hour at a temperature of about 1,100 °C, whereby a P-type well region 26 for forming channel having depth of 4 to 6 μm are formed. In this process, the energy for ion implantation is about 60 KeV, and the implaned quantity thereof is about $4x10^{13}$atoms/cm^2.

As shown in Fig. 2(F), the method further comprises the steps of effecting implantation of boron ion (B^+) from windows opened in the central portion of the upper surface of the well regions 26 with the resists 27 (shown by dotted line) serving as a mask, and removing the resist 27 upon completion of the ion implantation, whereby regions which will serve as P-type well contact regions are formed in the central portion of the well region 26. In this process, the energy for ion implantation is about 50 KeV, and the implanted quantity thereof is about $5x10^{15}$atoms/cm^2.

As shown in Fig. 2(G), the method comprises the steps of covering regions which will serve as P-type well contact regions with resists 28 (shown by dotted lines), and effecting ion implantation of phosphorus ion (P^+) with the resists 28 and the gate electrodes 25 serving as a mask. In this process, the energy for ion implantation is about 100 KeV, and the implanted quantity is $5x10^{15}$atoms/cm^2. The phosphorus ion is also entered

into the polysilicon layer 25.

Upon finishment of the above-mentioned steps, resists 28 are removed. Thus, the regions which will serve as a source region including a phosphorus ion (P+) are formed along the periphery of the regions which will serve as the well contact region.

As shown in Fig. 2(H), the method comprises the steps of forming an insulating film 29 essentially consisting of phosphoric glass in which molecular concentration of phosphorous (P) is about 3% and the thickness thereof is $7x10^2$nm (7,000A) so as to cover the whole surface, and effecting heat treatment in an atmosphere of nitrogen (N_2) at a temperature of about 1,050 C, whereby boron ion (B^+) and phosphorus ion (P^+) diffuse from the center to the periphery within the well region 26 to complete a P-type well contact regions 30 and N^+-type source regions 31 respectively.

Finally, as shown in Fig. 2(I), the method further comprises the steps of opening windows for the surface of the source region 31 and the well contact region 30 as well as windows for the leading-out port (not shown) of the gate electrodes, thereafter coating aluminum (Al) on the surface thereof by vacuum deposition so that the thickness thereof is 1.5 m, forming a source electrode 32 and an lead electrode for a gate (not shown) by etching, coating aluminum (Al) having the thickness of about 1 m on the lower surface of the drain substrate 20 of low resistivity by vacuum deposition, and alloying the aluminum at a temperature of about 450 C, thereby to form a drain electrode 33. Thus, the completed vertical-type MOSFET of the first embodiment is obtained.

In the processes according to the first embodiment, the N-type impurity, such as, arsenic is mixed or included in the silicon oxide film 23 embodded in the drain region 21 of high resistivity, and then the silicon oxide film 24 is formed on the surface of the drain region 21 of high resistivity. In these processes, N^+-type regions 23a of high impurity concentration are formed along the boundary portions between the oxide film 23 and

the drain region 21 of high resistivity by thermal diffusion. As a result, currents flow through the N^+-type regions 23a, thereby making it possible to reduce resistance which originates in the drain region of high resistivity to lessen "ON" resistance in current path.

Referring to Figs. 3, there is shown the second embodiment of the invention. A example of the fabricating processes of an n-channel vertical-type MOSFET according to the second embodiment will be described with reference to Figs. 3(A) to 3(H).

Initially, as shown in Fig. 3(A), the method comprises the steps of epitaxially growing an N^--type monocrystalline silicon layer 121 of low impurity concentration having donor concentration N_D of about $2x10^{15}$atoms/cm^3 and the thickness of about 15 m on a drain substrate 120 of low resistivity comprising an N^+-type monocrystalline silicon wafer of high concentration of donor impurities N_D of about $1x10^{18}$atoms/cm^3, thereby to form a drain region 121 of high resistivity, thereafter forming silicon nitride (Si_3N_4) film 123 on the surface of the drain region 121 of high resistivity of a semiconductor wafer 110 through a thin silicon oxide film 122 having the thickness of about 6x10 nm (600A) by a CVD method so that the thickness of the silicon nitride film 123 is about 10^2 nm (1,000A), and then removing silicon nitride film 123 except for portions in which a well regions functioning as channels are to be formed with resists 124 (shown with dotted lines) serving as a mask.

As shown in Fig. 3(B), the method comprises the steps growing an silicon oxide film by a thermal oxidation method on the removed portions to form oxide insulating film regions 125 having the thickness of about 1 m, then removing the silicon nitride films 123 and the resists 124 using phosphoric acid, at the same time removing the thin oxide film 122 located at the lower surface of the silicon nitride film 123, and thereafter forming a silicon oxide insulating film 126 for a gate on the surface of the drain region 121 of high resistivity except for

the thick oxide film region 125 by a thermal oxidation method so that the thickness thereof is about 10^2 nm (1,000Å). In the process of growing the thick oxide insulating film region 125, each peripheries of the region 125 grows in the upper and lower directions in such a manner as to push up the peripheral portion of the silicon nitride film 123. Accordingly, the thick oxide insulating film regions 125 are formed in such a manner that each upper part is projected with respect to the surface of the insulating film 126 for a gate. More particularly, the oxide insulating films 125 are trapezoid-shaped in appearance, which have gradually inclined peripheral edges, respectively.

As shown in Fig. 3(C), after the selective oxidation process is completed, the method further comprises the steps of forming a polysilicon film 128 having the thickness of about 4×10^2nm (4,000Å) by a CVD method, selectively removing the polysilicon film by photo-etching techniques with resists 127 serves as a mask so that gate electrodes 128 are left, and injecting boron ions (B^+) into the portions in which there exist no gate electrode 128 on the upper surface of the drain region 121 of high resistivity by an ion implantation method with the gate electrodes 128 serving as a mask. The energy for ion implantation is about 60 KeV, and the implanted quantity is about 4×10^{13}atoms/cm^2.

As shown in Fig. 3(D), the method further comprises effecting heat treatment for 24 hours at a temperature of about 1,100 °C thereby to form well regions 129 having the depth of 5 to 6μm by diffusion, and injecting boron ions (B^+) into a predetermined surface of the well regions 129 with the resists 130 (shown with dotted lines) serving as a mask. The energy for ion implantation is about 50 KeV, and the implanted quantity is 5×10^{15}atoms/cm^2.

As shown in Fig. 3(E), the method further comprises the steps of covering with resists 131 the regions into which the boron ions (B^+) have been injected in the preceding step, and then injecting phosphorus ions (P^+) into the surface of the well

region 129 with the resists 131 and the gate electrodes 128 serving as masks. In this instance, a great amount of phosphorus ions (P^+) are immersed into the polysilicon films constituting the gate electrodes 128. The energy for ion implantation is about 100 KeV, and the implanted quantity is about $5x10^{15}$atoms/cm^2.

As shown in Fig. 3(F), after the above-described ion implantation is completed, the method further comprises the steps of forming an insulating film 132 essentially consisting of phosphoric glass having molecular concentration of about 3% by a CVD method so that the thickness thereof is $7x10^2$nm (7,000A), and effecting heat treatment in the presence of a current of nitrogen at a temperature of about 1,050 C, whereby source regions 133 and well contact regions 134 are formed within the well region 129 by thermal diffusion.

As shown in Fig. 3(G), after the double diffusion process described above is completed, the method further comprises the steps of opening windows exposed to the surface of the source regions 133 and the well contact region 134 as well as windows for the leading-out port (not shown) of the gate electrodes, then coating aluminum of about 1.5 m in thickness by vacuum deposition, thereafter forming source electrode 135 and lead electrodes for a gate (not shown) by etching, coating aluminum having the thickness of 1 m on the rear surface of the drain substrate 120 of low resistivity by vacuum deposition, and then effecting heat treatment at a temperature of about 450 C, whereby an alloy drain electrode 136 is formed. Thus, the vertical-type MOSFET shown in Fig. 3(G) of the second embodiment is completed.

According to the second embodiment, in the selective oxidation process shown in Fig. 3(B) the peripheral portion of the thick oxide insulating film region 125 rises so as to be gradually sloped surface. Accordingly, when the gate electrode 128, the insulating film 132 and the source electrode 135 are successively stacked, there occurs no crack between respective layers due to the offset structure by the gentle slopes thereof.

Further, the stress applied to each films of the layers can become substantially uniform throughout whole portion of each film.

Further, in the selective oxidation process shown in Figs. 3(A) and 3(B) in the second embodiment, another method may be employed, which comprises the steps of effecting arsenic ions (As) implantation with a resist 124 serving as a mask into the surface of the drain region 121 of high resistivity, and then forming a thick oxide insulating film region 125 in the same portions as stated above.

The arsenic ions (As) thus implanted forms an N^+-type region of high impurity concentration along the interface between the insulating film region 125 and the drain region 121 of high resistivity by thermal diffusion in Fig. 4(G). Accordingly, similar to the first emboddiment, electric currents flow through the N^+-type region, thereby making it possible to reduce resistance which originats in the drain region of high resistivity to lessen "ON" resistance in current paths.

Referring to Fig. 4, there is shown the third embodiment of the invention. An example of fabricating processes of an N-channel vertical type MOSFET according to the third embodiment will be described with reference to Figs. 4(A) to 4(H).

Initially, as shown in Fig. 4(A), the method comprises the steps of epitaxially growing an N^--type monocrystalline silicon layer of low impurity concentration having donor concentation N_D of about $2x10^{15}$atoms/cm^3 and the thickness of about 15μm on a drain substrate 220 of low resistivity essentially consisting of an N^+-type monocrystalline silicon wafer of high impurity concentration having donor concentration N_D of about $1x10^{18}$atoms/cm^3 thereby to form a drain region 221 of high resistivity, forming a silicon oxide insulating film 222 for a gate on the surface of the drain region 221 of high resistivity of a semiconductor wafer 210 by a thermal oxidation method so that the thickness thereof is about 10^2nm (1,000Å), thereafter forming a polysilicon film 223 having the thickness of $4x10^2$ nm

(4,000A) by a CVD method and forming a silicon nitride film (Si_3N_4) 224 on the surface thereof by a CVD method so that the thickness thereof is about 10 nm (1,000A).

As shown in Fig. 4(B), the method further comprises the step of selectively removing the silicon nitride film 224 with resists 225 (shown with dotted lines) serving as masks. The removed portions of the film 224 correspond to the portions of the drain region 221 that is to interpose between two well regions and the portions that is to be source regions.

As shown in Fig. 4(C), the method further comprises the step of oxidizing the polysilicon films 223 except for the gate electrode portions by thermal oxidation to change them into silicon oxide films 226. In this oxidation process, the silicon oxide insulating film 226 grows in a manner to push up the opened inner peripheral edge in the window provided in the silicon nitride film 224. Accordingly, the insulating films 226 rise on the surface so as to have trapezoidal shape in cross section.

As shown in Fig. 4(D), after the above-mentioned selective oxidation process is finished, the method further comprises the steps of removing the silicon nitride film 224 by photo-etching techniques, selectively removing the polysilicon oxide insulating films 226 which coat the portions in which the well regions will be formed, covering the upper surface of the gate electrodes 223 and the insulating films 226 with resists 227 (shown with dotted line), and injecting boron ions (B^+) into the surface of the drain region 221 of high resistivity by an ion implantation method under the condition that the gate electrode 223 and the resist 227 serve as a mask. The energy for ion implantation is about 60 KeV, and the implanted quantity is about $4x10^{13}$atoms/cm^2.

As shown in Fig. 4(E), the method further, comprises the steps of effecting heat treatment for 24 hours at a temperature of 1,100 C to form P well regions 228 by thermal diffusion, and injecting boron ion (B^+) into the surface of the well region 228 from windows opened in the center thereof with the resists 229

serves as masks. The energy for ion implantation is about 50 KeV, and the implanted quantity is about $5x10^{15}$atoms/cm^2.

As shown in Fig. 4(F), the method further comprises the steps of covering the region into which the boron ions are injected at the preceeding process with resists 230, and injecting phosphorus ion (P^+) into the well regions 228 with the resist 230, the silicon film 223 and the insulating film 226 serving as a mask. In this instance, a great amount of phosphorus ions are entered into the gate electrode 223. The energy for ion implantation is about 100 KeV, and the implanted quantity is about $5x10^{15}$atoms/cm^2.

As shown in Fig. 4(G), the method further comprises the steps of forming an insulating film 231 essentially consisting of phosphoric glass, the molecular concentration of phosphorus being about 3%, by a CVD method so that the thickness thereof is $7x10^2$nm (7,000A), and effecting heat treatment in the atmosphere of nitrogen at a temperature of about 1,050 C, whereby source regions 232 and well contact regions 233 are formed within the well region 228 by thermal diffusion.

Finally, as shown in Fig. 4(H), after the thermal diffusion process is finished, the method further comprises the steps of opening windows in the insulating films 222, 231 for forming electrodes on the source regions 232 and well contact regions 233, opening window in the insulating film 231 for leading-out ports of gate electrodes (not shown), coating aluminum on the whole surface thereof by vacuum deposition so that the thickness thereof is 1.5 m, forming a source electrode 234 and a lead electrode (not shown), for a gate by etching, thereafter coating aluminum having the thickness of about 1 m on the whole rear surface of the wafer 210 by vacuum deposition, and alloying it at a temperature of about 450 C thereby to form a drain electrode 235. Thus, the vertical MOSFET of the third embodiment shown in Fig. 4(H) is completed.

In the selective oxidation process shown in Fig. 4(C), the oxide insulating film 226 rises so as to be gradual inclined at

its surface. In the case where the insulating film 231 and the source eletrode 234 are successively stacked as described above and illustrated in the figures, there occurs no crack between layers due to offset structure by the gentle slopes thereof. Further, the stresses applied to the films of each layers can became substantial uniform as well as the thicknesses thereof.

In the selective oxidation process shown in Figs. 4(C), similar to the second embodiment, another method may be employed, which comprises the steps of injecting an N-type impurity, such as phosphorus ions (P^+) into the silicon policrystalline 223 with the resists 225 by an ion implantation method in advance. As described above the MOS transistor produced according to this method makes it possible to reduce resistance due to the drain region of high resistivity, thereby to lessen resistance in current paths when the element is switched on.

In the above-mentioned embodiments, the P-type well region is formed on the N-type substrate. However, the present invention is applicable to a P-channel vertical-type MOSFET that an N-type well region is formed on a P-type substrate.

As appreciated from the detailed description in connection with the preferred embodiments, the vertical-type MOSFET according to the present invention is constituted so as to increase the effective distance between the gate electrode film and the drain region in the central portion of the gate electrode film located between adjacent well regions for forming a channel. Accordingly, this makes it possible to remarkably decrease feedback capacity between the gate and the drain, thereby to effect switching at a high speed.

<u>What is claimed is;</u>

1. A vertical-type MOSFET comprising;

a semiconductor wafer functioning as drain,

a drain electrode joined to the lower surface of said wafer,

a plurality of a well regions formed in the upper side of said wafer apart from each other,

a plurality of source regions each of which is formed in one of said well region respectively,

a gate electrode formed on said adjacent well regions and said wafer interposed therebetween through a gate insulating film in a manner that the distance between said gate electrode and central portion of said interposed portion of said wafer that functions as drain region is larger than the distance between said gate electrode and said well region,

a source electrode electrically contacting to said source regions.

2. A vertical-type MOSFET claimed in claim 1, wherein,

said film is locally thicker at the part corresponding to said central portion of said wafer than that of other part.

3. A vertical-type MOSFET claimed in claim 2, wherein, said thicker film rises so as to form a gentle sloped surface on said wafer.

4. A vertical-type MOSFET claimed in claim 1, further comprising insulators positioning between said central portions of said wafer and said gate electrodes so that the distance between said gate electrode and said central portions of said wafer is larger that the distance between said gate electrode and said well regions.

5. A vertical-type MOSFET comprising;

a semiconductor wafer functioning as drain,

a drain electrode joined to the lower surface of said wafer,

a plurality of well regions formed in the upper surface of said wafer apart from each other,

a plurality of source regions each of which is formed in said well region,

a gate electrode formed on said upper surface of said wafer through gate insulating film,

a insulator interposed between said adjacent well regions apart from said adjacent well regions,

said insulator formed by thermal oxidation of said gate electrode,

a source electrode formed on said source rgions.

6. A vertical-type MOSFET claimed in claim 5, wherein,

said insulator rises so as to form a gentle sloped surface on said wafer.

7. A method of fabricating a vertical-type MOSFET comprising;

(A) step of forming an silicon oxide film on the upper surface of a semiconductor wafer in a manner that the thickness of the portions thereof which is to interpose between adjacent well regions is thicker than that of other portion,

(B) step of forming gate electrodes on said silicon oxide film,

(C) step of forming said well regions by ion implantation method with said gate electrodes functioning as a mask,

(D) step of forming source regions in said well regions with said gate electrodes functioning as a mask,

(E) step of forming source electrodes on said source regions and drain electrode on a lower surface of semiconductor.

8. A vertical-type MOSFET claimed in claim 7, wherein,

said interposed portion of said silicon oxide film is formed so as to rise from said wafer forming a gentle sloped surface.

9. A method of fabricating a vertical-type MOSFET claimed in claim 7, wherein,

said silicon oxide film is formed in a manner that said interposed portions includes therein impurities of the conductivity type corresponding to that of said wafer at the step (A).

10. A method of fabricating a vertical-type MOSFET comprising;

(A) step of forming recess portions on an upper surface of a semiconductor wafer,

(B) step of depositing insulators in each of said recess portions,

(C) step of forming a silicon oxide film and a polysilicon layer on the whole upper surface of said semiconductor wafer in the manner that said polysilicon layer is insulated from said wafer by said silicon oxide film and said deposited insulator,

(D) step of selectively removing the portions of said polysilicon layer corresponding to the portions of said wafer in which source regions are to be formed,

(E) steps of effecting ion implantation in said portions of said wafer corresponding to said removed portion and forming well regions by a heat treatment,

(F) steps of effecting ion implantation in said portions of said wafer corresponding to said removed portion and forming source regions by a heat treatment,

(G) step of forming source electrodes on said source regions and drain electrode on a lower surface of said wafer.

11. A method of fabricating the vertical-type MOSFET claimed in claim 10, wherein,

said insulator deposited in said recess portion includes therein impurities of the conductivity type corresponding to that of said wafer.

12. A method of fabricating a vertical-type MOSFET comprising,

(A) step of forming a silicon oxide film and polysilicon film stacked said silicon oxide film on the upper surface of a silicon wafer,

(B) step of selectively oxidizing said polysilicon except for gate electrodes, said oxidized portions of said polysilicon includes the portion that is to interpose between adjacent well regions apart from said adjacent well regions,

(C) step of removing said oxidized portions facing to the portion of said wafer that is to be source regions,

(D) step of forming said well and source regions, said source region formed in said well region,

(E) step of forming source electrodes on said source

regions and drain electrode on the lower surface of said wafer.

13. A method of fabricating a vertical-type MOSFET claimed in claim 12, wherein,

said well and source regions is formed by ion implantation method and thermal diffusion and said interposed portion of said oxided polysilicon is doped with impurities of the conductivity type corresponding to said wafer prior to said thermal diffusion.

FIG. 1
PRIOR ART

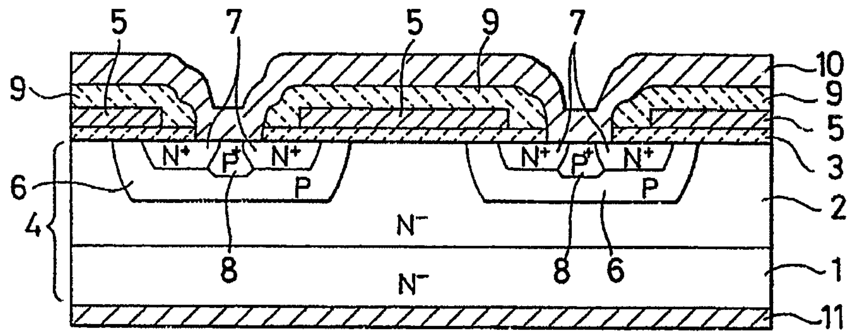


FIG. 2(A)

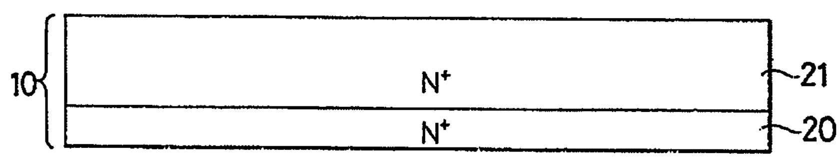


FIG. 2 (B)

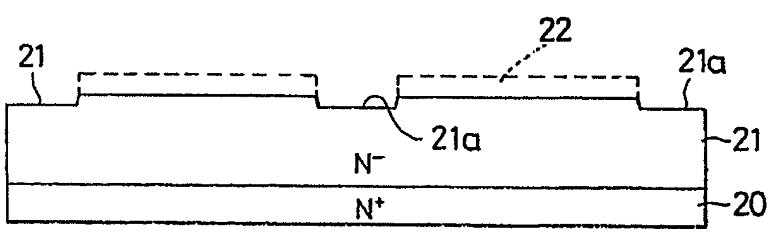


FIG. 2 (C)

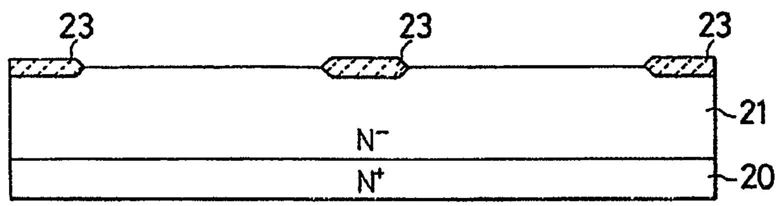


FIG. 2 (D)

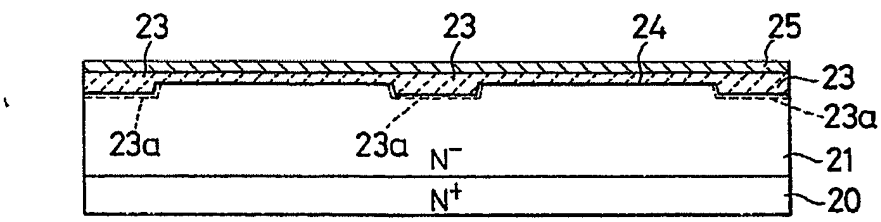


FIG. 2 (E)

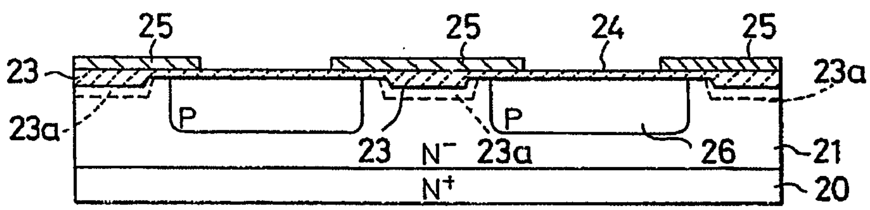


FIG. 2 (F)

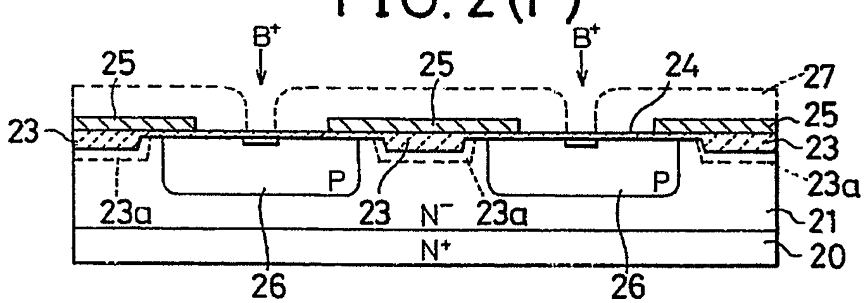


FIG. 2 (G)

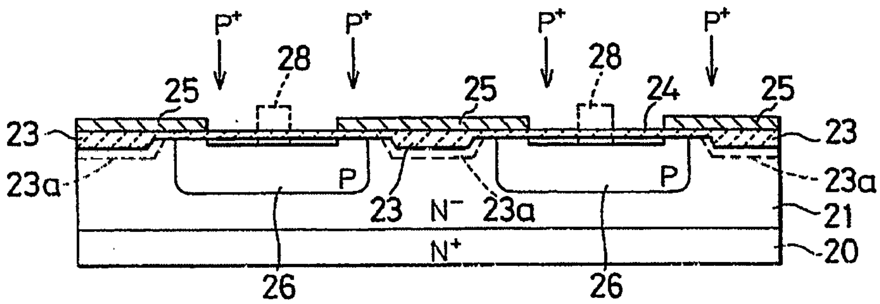


FIG. 2 (H)

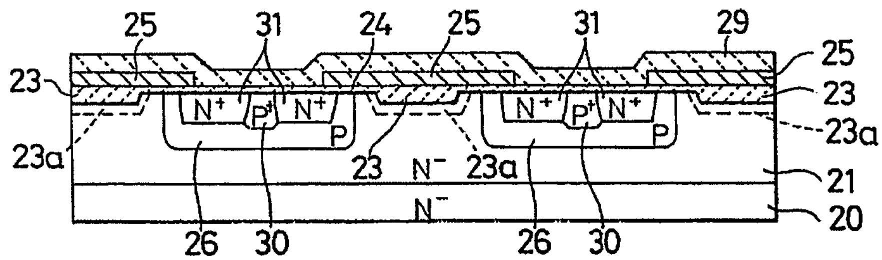


FIG. 2 (I)

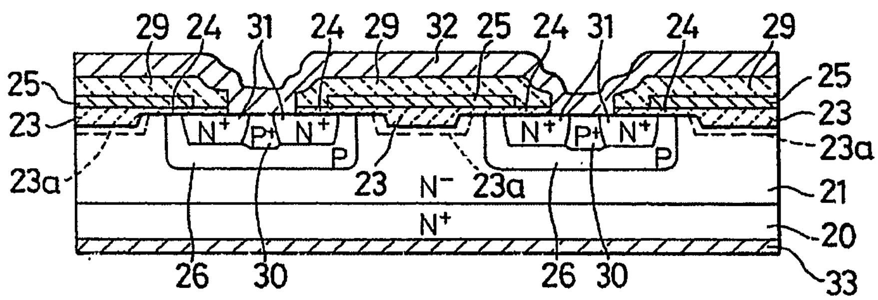


FIG. 3(A)

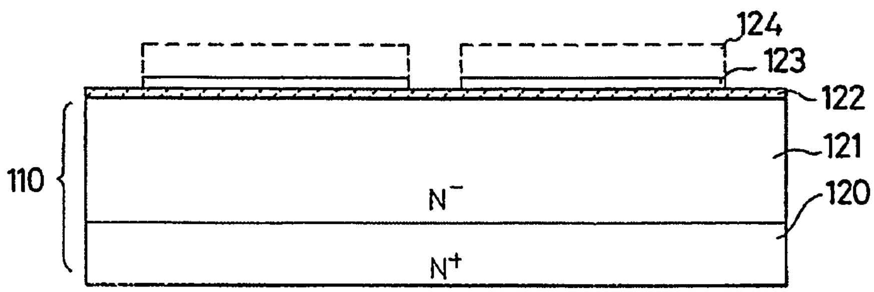


FIG. 3(B)

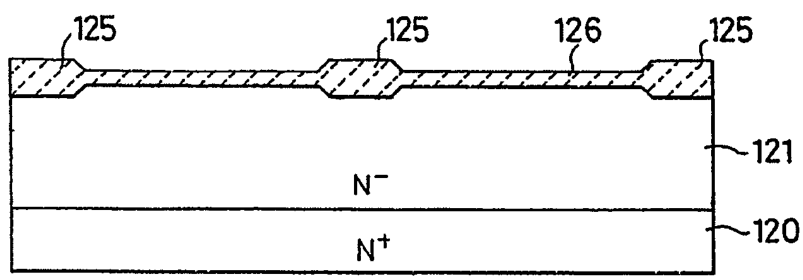


FIG. 3(C)

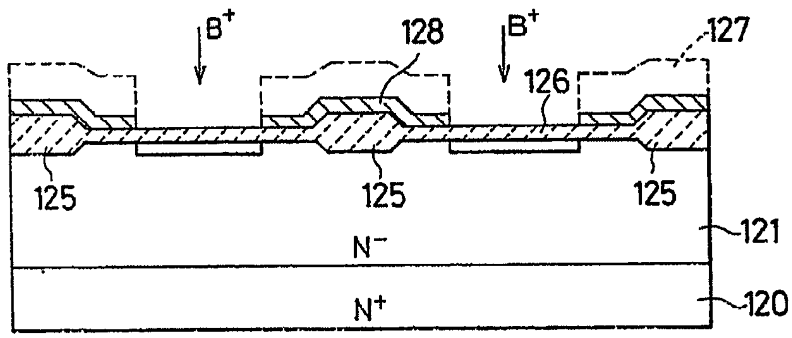
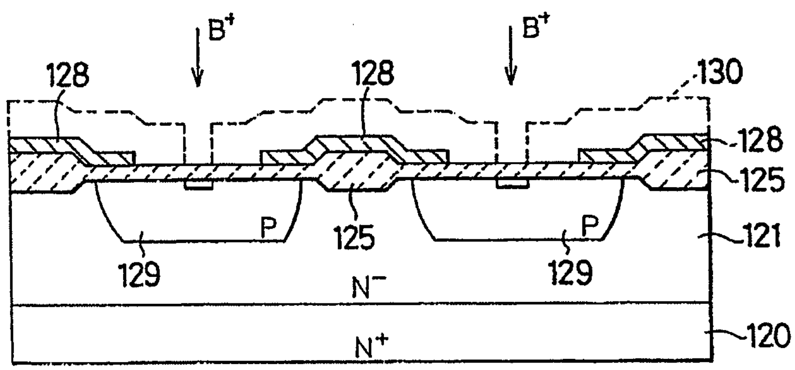

B+
128
B+
127
126
125
125
125
121
N−
N+
120

FIG. 3(D)


B+
B+
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P
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121
129
129
N−
N+
120

FIG. 3(E)

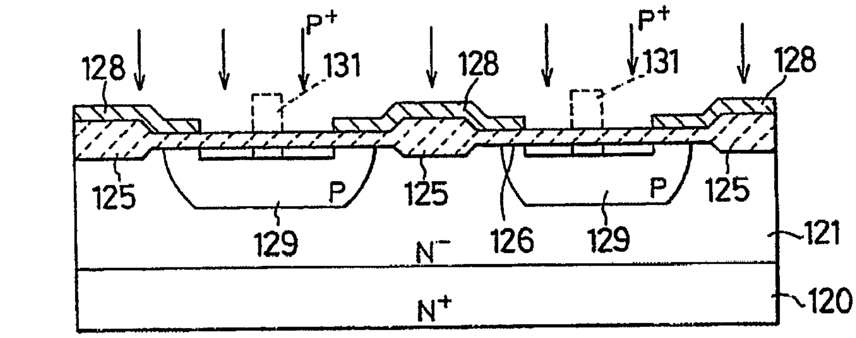


FIG. 3(F)

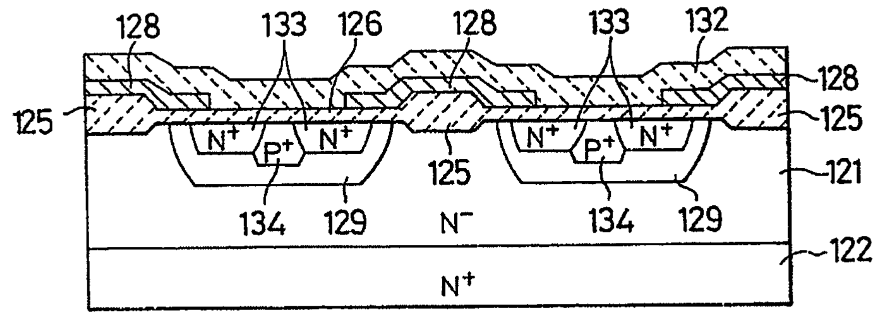


FIG. 3(G)

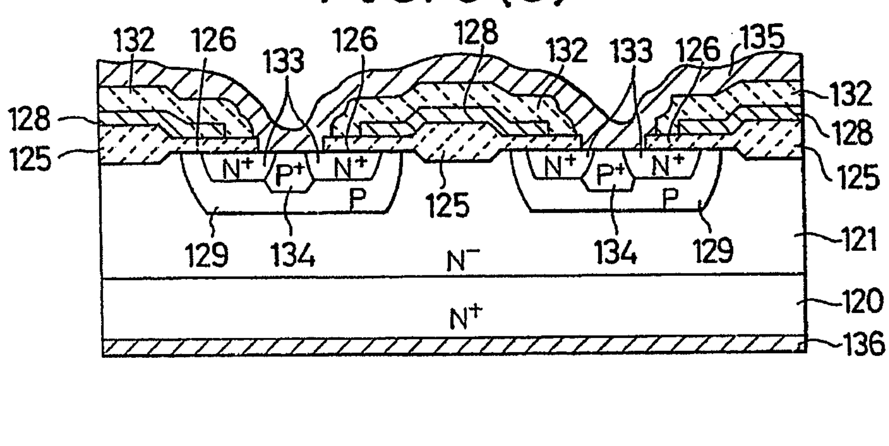


FIG. 4(A)

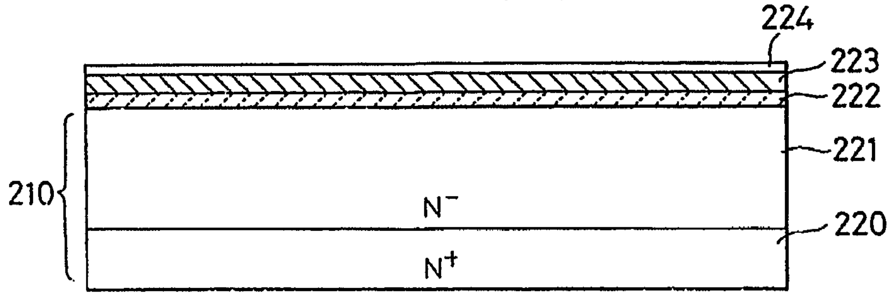


FIG. 4(B)

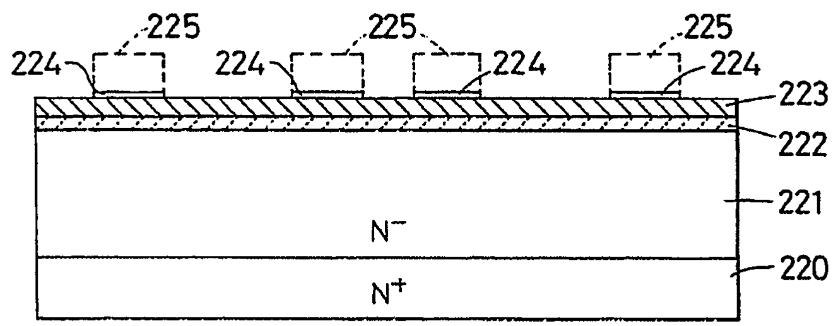


FIG. 4(C)

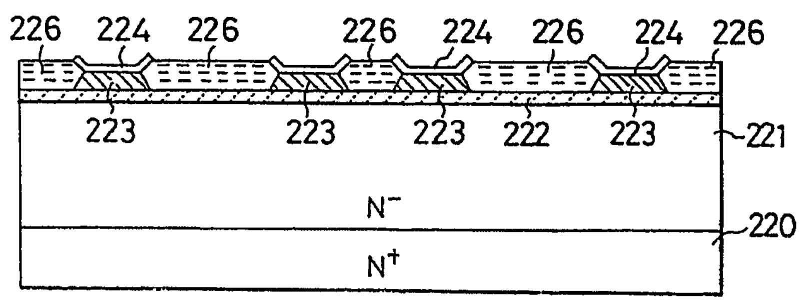


FIG. 4(D)

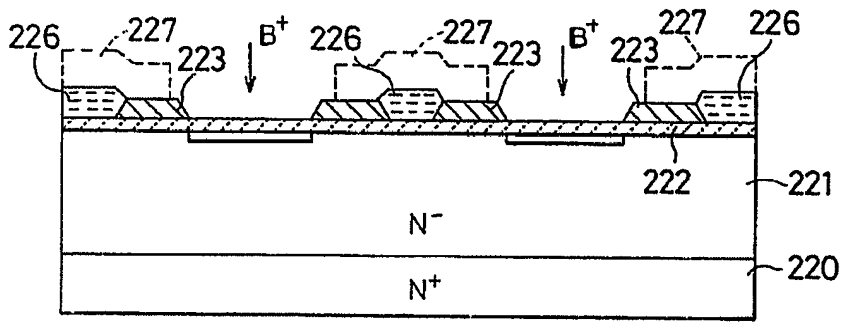


FIG. 4 (E)

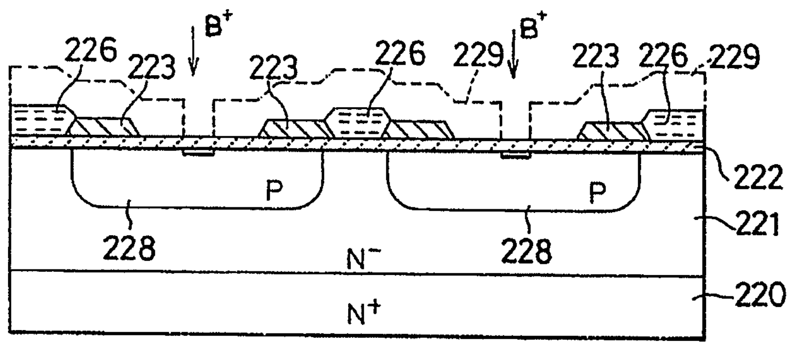
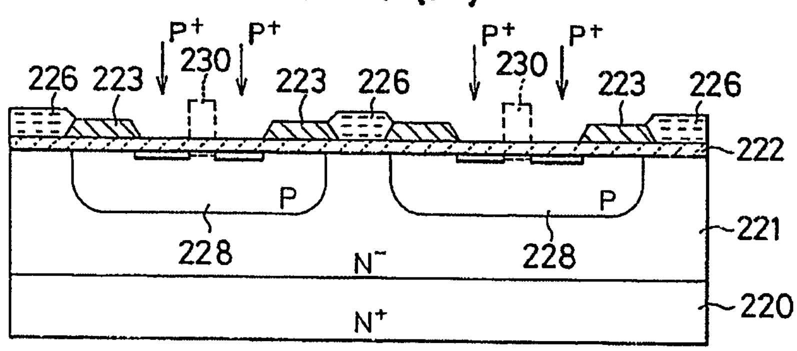
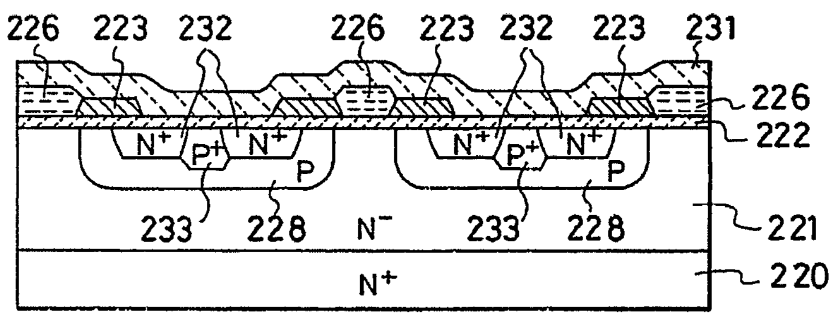


FIG. 4(F)



F I G. 4 (G)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N+
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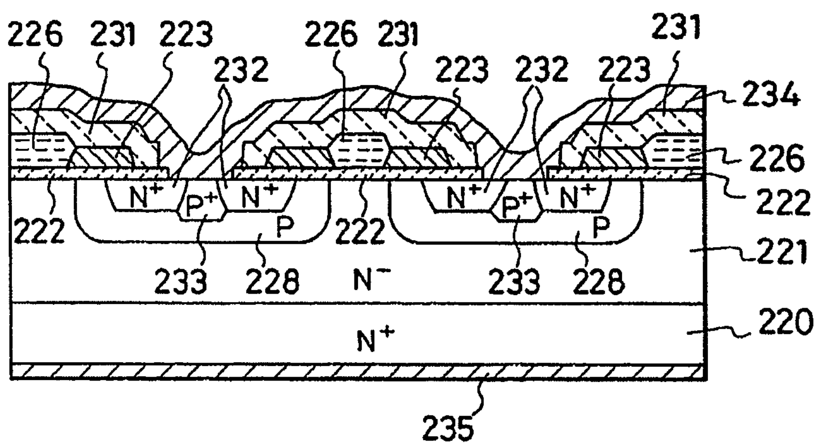
228
N−
233
228
221
N+
220

F I G. 4 (H)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P+
N+
P
221
233
228
N−
233
228
N+
220
235

0119400

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EUROPEAN SEARCH REPORT

Application number

EP 84 10 0612

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 3)
			H 01 L 29/78
A	FR-A-2 476 914 (RCA CORP.) * Page 2, line 28 - page 3, line 22; figure 1 *	1,5	
A	DE-A-3 114 972 (SUPERTEX, INC.) * Claims 1-12; figures 1,4,6 *	1,5	
A	GB-A-2 062 349 (RCA CORP.) * Claims 1-24 *	1,5,7, 10,12	
A	US-A-4 072 975 (A. ISHITANI) * Column 4, line 38 - column 6, line 38; figures 4A-4I *	7,10, 12	
	-----		TECHNICAL FIELDS SEARCHED (Int. Cl. 3)
			H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	09-05-1984	ZOLLFRANK G.O.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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